ACTIVITIES UNLIMITED

- SCIENCE AND TECHNOLOGY CLUB
- COMPUTER CONCEPTS—
- HARDWARE HISTORY AND OPERATION
- AVIONICS APPLICATION

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COMPUTER CONCEPTS

- Mechanical Computers
  Electronic Computers
  Turing's Universal Machine
- Harvard Architecture-
  Block Diagram Discussion
  General Purpose Computers vs. 'Programmable Controllers'
  Typical Computer Instruction Set -Assembly Language (80xx)
- Communication with Program-
  PIO, INT, DMA
- Microcomputer (uP) Semi-Conductor Technology Development
- Computer History/Timeline—Available from Internet-Pictures etc.
  Moore's Law
  Future Developments

MECHANICAL COMPUTING CONCEPTS

- **ANCIENT**
  ABACUS (2,500 YEARS AGO)
  GREEK/ROMAN- ANTIKYTHERA

- **RENAISSANCE TIME**
  Scientists used Tables to perform calculations more rapidly. Unfortunately, human error limited the usefulness of the Tables. Schickard (1592-1630), Pascal (Count 'sums of money'), Leibintz (More reliable device-Calculus) developed machines to calculate tables.

MECHANICAL COMPUTING CONCEPTS

- **1800S**
  Babbage-General Purpose 'Analytic Engine'-Not able to be built.
  Hollerith –Punch Cards— Engineer in Census Bureau—Started his own Company and obtained contract for 1890 US Census.
- **1900S**
  IBM-Office Equipment
  Marchand-Mechanical Add/Mult/Divide
- **TURING'S 'UNIVERSAL MACHINE' CONCEPT**
- **MECHANICAL COMPUTERS**

  Limited Capability-Too difficult to design & fabricate for modern requirements.

ELECTRONIC COMPUTING CONCEPTS

- **VON NEUUMAN'S STORED PROGRAM CONCEPT**
  He identified 'Organic' Computer sections-
  Arithmetic, Storage, Control, Human Interface and he recognized that the Instructions could be contained in the same Memory as Data & Intermediate Results.

- **HARVARD ARCHITECTURE**
  Contains CPU, Instruction & Data Memory, Control & Timing, I/O.
  Information flows In & Out of Memory via CPU, potential 'Bottleneck'.
  Criticized for 50 years, but no serious challengers-appears to be an elegant, 'natural' Configuration.

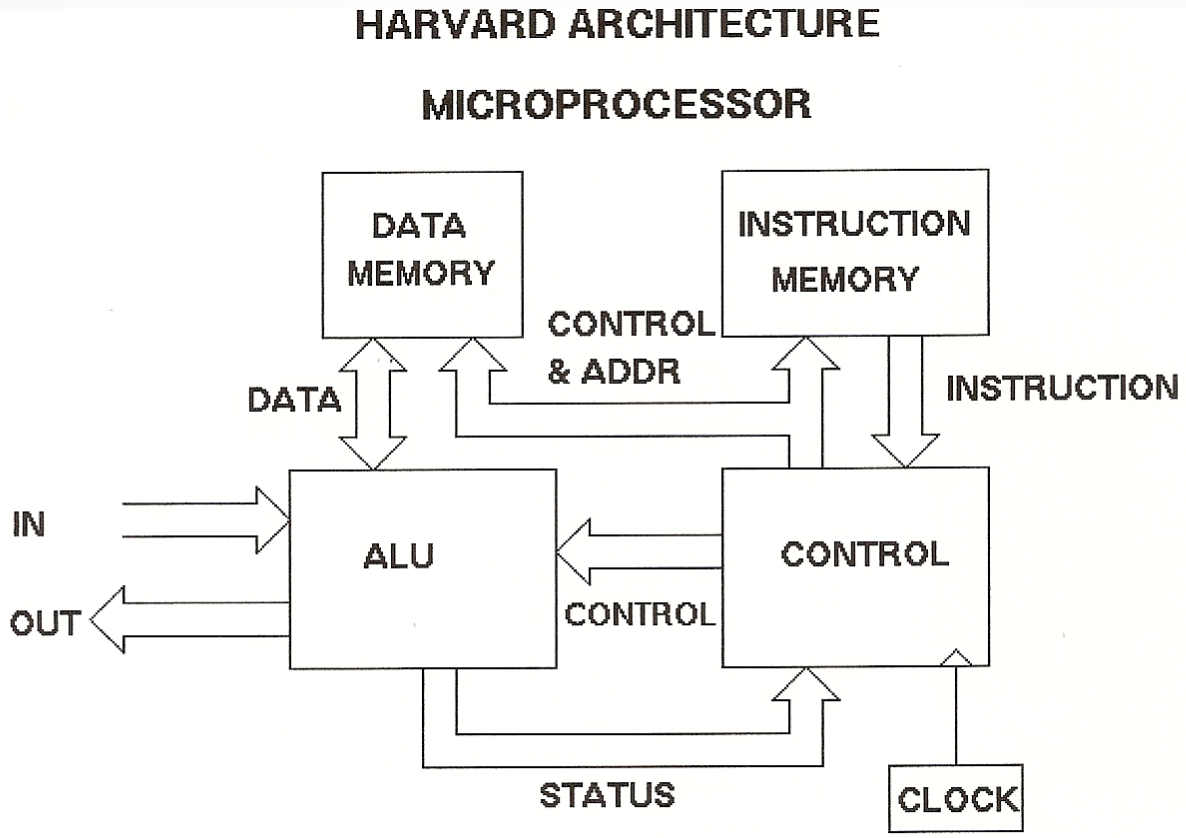
BLOCK DIAGRAM/ COMPUTER MICRO-PROGRAM DISCUSSION

- **COMPUTER PROGRAM COUNTER**
  The Computer Program Counter (PC) is Initialized at 'Power turn-on' to Zero & 'steps through' the Program Instructions which are contained in the Instruction Memory (IM). Each Count forms the Address of an Instruction in the Instruction Memory. At Final (Terminal) Count, the Counter 'Overflows' and returns to Zero.

BLOCK DIAGRAM/ COMPUTER MICRO-PROGRAM DISCUSSION

- **INSTRUCTION REGISTER (IR)**
  Since time is required to execute Instructions, as each Instruction is 'Read' out to the IM, it is coupled to the IR which is provided for temporary storage of the Instructions, which are then 'Routed' to the Micro-Program Read Only Memory (ROM). The 'Bit' pattern of each instruction is different, with certain fields or sections used to form a specific address to the Micro-Program Read Only Memory (ROM). The outputs of the ROM are the Micro-Instructions employed to control the 'Micro-Program Controller'.

HARVARD ARCHITECTURE MICROPROCESSOR BLOCK DIAGRAM



BLOCK DIAGRAM/ COMPUTER MICRO-PROGRAM DISCUSSION (CONT'D)

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BLOCK DIAGRAM/ COMPUTER MICRO-PROGRAM DISCUSSION (CONT'D)

- **THE MICRO-PROGRAM CONTROLLER**

  The Micro-Program Controller is essentially a 'Processor-within-a-Processor', whose functions are 'tailored' to the specific internal Processing Functions of the CPU etc. Thus, in the same sense that the main Computer Program is 'stepped through' by the Computer Program Counter (PC), the Micro-Program Controller 'steps through' the Micro-Instructions.

- **COMPUTER CYCLE COUNTER**

  Since there are 'multiple sub-steps' in the Micro-Instructions which take place sequentially, a Computer Cycle Counter (CC Counter) is provided to 'step through' these various portions of the Micro-Program. For example, if the Instruction is Read Data from the Data Memory, and transmit it to the CPU for processing, the first part of the Instruction is to 'Fetch' the data, with the next part to 'Write' the Data to the Arithmetic Logic Unit (ALU). Finally, the ALU performs the required operations.

  As indicated, these "steps' of the Micro-Instruction program are performed sequentially.

TYPICAL COMPUTER INSTRUCTION SET/ CISC/RISC UPS

- **GENERAL PURPOSE (GP) COMPUTERS**

  Computers employ Instructions of various types to perform specific functions as related to the computer's application. For 'General Purpose (GP) Computers', the Instructions must be well formulated to satisfy multiple applications, and the GPs are generally programmed utilizing Higher Order Languages (HOLs).

  In addition to GPs, many applications can be satisfied by 'Programmable Controllers' which are 'Hardware' type Electronic devices requiring very specific Instructions which were contained in a Memory Chip, as a separate part of the Programmable Controller.

TYPICAL COMPUTER INSTRUCTION SET/ CISC/RISC UPS (CONT'D)

These instructions employ short Mnemonics to represent the processing operations that related to Hardware commands (Turn-On/Off Switch etc.) and are written at the Assembly Language Level.

The development of Microprocessors containing the Instruction Memory which is integrated into the Silicon Chip, required formulation of Instruction types which would provide 'Programming Flexibility', but not compromise Computing performance.
INTEL developed the 80XX family of 147 instructions called the **Complex Instruction Set Computer (CISC)** Instructions. These were well received by Programmers, but were considered to be 'Performance Limited', since many of the Instructions contained 'sub-instructions' each requiring Machine Cycles (time) to be executed. This led to the development of **Reduced Instruction Set Computer** (RISC) Computers, which completed each instruction in a single Machine Cycle, but required multiple cycles to perform the equivalent CISC Instruction.

TYPICAL COMPUTER INSTRUCTION SET/ CISC/RISC UPS (CONT'D)

- While some RISC UPS were made, INTEL resisted this development because of its 'backward/forward' software compatibility concerns. Improved Semi-conductor technology eventually led to the PENTIUM family which 'transparently' combined RISC instructions into CISC, while maintaining performance and S/W compatibility.
- Improved Software Development Tools (Compilers etc.) eventually permitted programmers to readily 'Code' both type Microprocessors.
  Note that the Assembly Level 80XX Instructions are extremely tedious and difficult to use and may require Engineering Oriented Programmers. Complex Electronic Systems (Navigation, Control, Communication etc.) programs are usually required to be written in HOL but can contain Assembly Language Instructions for critical timing operations.

TYPICAL COMPUTER INSTRUCTION SET/ CISC/RISC UPS (CONT'D)

- TYPICAL UP INSTRUCTION SET.

  8086 FAMILY INSTRUCTIONS:

  CLR- CLEAR, CARRY

  CMP- COMPARE

  SAR-SHIFT ARITHMETIC RIGHT.

COMMUNICATION WITH THE COMPUTER PROGRAM

- **Basic computer operation** involves repetitive execution of a specific program.
  In order to provide controls which facilitate operation with the outside world various functions are employed:
- **Programmed Input Output Control (PIO)--**
  Periodically data from the External World can flow In or Out of the Computer data memory, but the action does not change the repetitive program operation.
- **Interrupt/Acknowledge (Int/Ack)--**An Interrupt Service Routine (ISR), which is not part of the normal program execution, allows data from the External World to flow In or Out of the Computer Program.
- **Direct Memory Access (DMA)–** The Computer Program is Halted, and the I/O can send Data Directly in/out of the Computer Memory (requires additional circuitry).

MICRO-COMPUTER SEMI-CONDUCTOR TECHNOLOGY DEVELOPMENT/ GENEALOGY

- Transistor Feature Size has been reduced by a Factor of approximately 300,000 in 35 years, with the numbers of transistors increased dramatically!! Follows Moore's Law closely.
- **DATE MNF'R MODEL # TRANSISTORS**

1971	INTEL	8008	3,300
1979	INTEL	8088	29,020
1981	MOT	68000	68,000
1985	INTEL	80386	275,000
1987	MOT	68030	273,000
1993	INTEL	PENTIUM	3.1 MILLION
2000	INTEL	PENTIUM 4	42 MILLION
2005	INTEL	DUAL PROC	1 BILLION

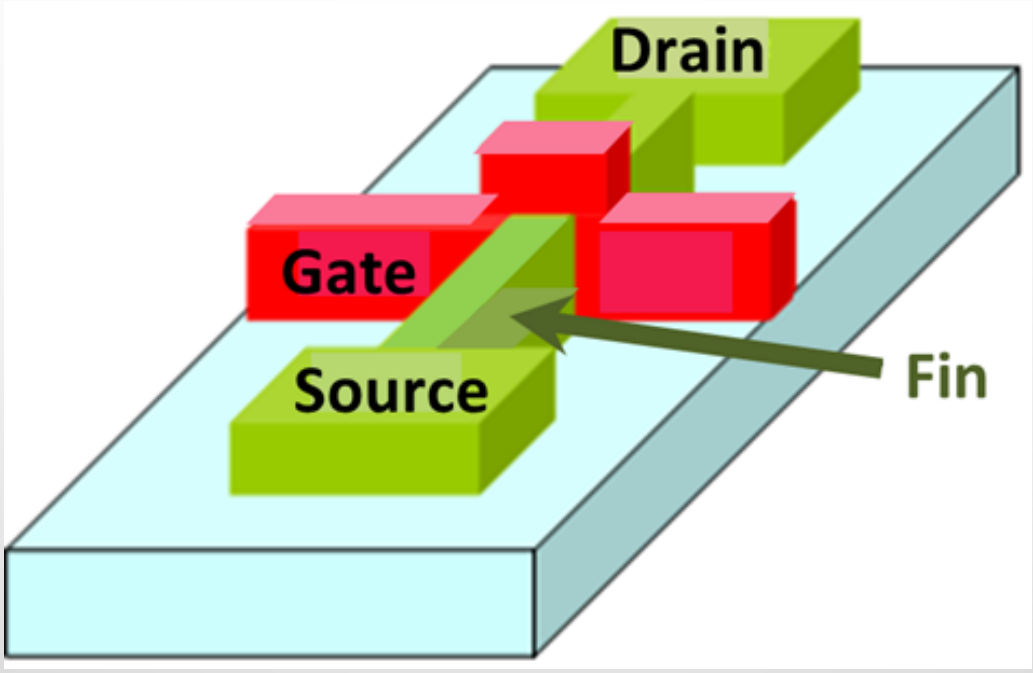
SEMICONDUCTOR DEVELOPMENT UPDATES

- **MOORE'S LAW** was originally established to indicate the Circuit Density improvements in microprocessor chips-- A factor 5.9 Million Times in 45 years.
- TODAY THE **AMD ZEN2,** is the largest transistor count in a commercially available microprocessor --39.54 billion MOSFETs--8 dies in a single package!!
- In 2019, the highest transistor count is in a non-memory chip, called the **Wafer Scale Engine 2** by Carebras. It has 2.6 trillion MOSFETs and is manufactured by TSMC using their 7 nm process.

SEMICONDUCTOR DEVELOPMENT UPDATES

- By 2003, shrinking Planar (2 dimensional) transistors was limited to 45nm. In order to continue Density improvements, **'FINFETS'** were developed--so named because they appear to be similar to 'Fish-fins' protruding from the Planar Surface. In addition to density improvements, this three-dimensional design also solves the Semiconductor Thermal limit problem caused by Transistor 'OFF Leakage.
- Synchronization between processors, or any multiple computer configuration is always an issue. Cloud computing with devices all over the world forming Supercomputers operating on specific massive problems continues to be improved.

FINFET PHOTO



B2 PHOTO

AVIONICS APPLICATION

- **AVIONICS APPLICATION B2 ADVANCED TECHNOLOGY, STEALTH BOMBER**
  - Aircraft was developed in the 1980's to penetrate soviet air defenses, deliver nuclear weapons, and return to US Bases. It includes a self-contained Observatory to permit guidance by use of Star Sighting (extensive catalog) and return to any based selected.

AVIONICS APPLICATION

- Stealth technology was demonstrated with the success of the F117 Fighter developed by Lockheed in the Skunk Works.
- In order to direct radar energy in the least revealing directions, its external shape incorporates large radius curved surfaces. No vertical fin stabilizers are used, so flaps on the trailing edges of the wings are provided to control roll, pitch, and yaw.
- Sophisticated artificial stabilization (Attitude Motion Detector Systems-- AMSS) (Rate gyro) and, control systems to provide satisfactory flying characteristics. Note that the B2 is extremely 'Stealthy' to observers on the ground because engine exhaust is from the top of the aircraft. As satellite monitoring systems were developed, heat from the exhaust becomes observable.

AVIONICS APPLICATION

- While the original plan was for an aircraft named for each state, but only 21 B2s were built. They have been rarely used but are extremely effective. They are now 30 years old, and are continually upgraded for additional missions- bunker buster bombs, ALCM etc.

- **B2 Aircraft Crew Size**

  The B2 was designed to need a crew of only 2- pilot and weapons systems engineer. The previous US Air Force Bombers required a crew of 5. The technology to accomplish the reduction was formidable and expensive but justified.

AVIONICS APPLICATION

- This reduction was to be accomplished by massive use of Computers and Microprocessors –more than 250, many of which performed 'embedded', never changing hardware type functions.
- However, the Government (1980s) had been 'exploited' many times, where purchase and programming of a computer was obsolete before it was completed. They thus imposed requirements, to add documentation and computer support which, while necessary for general purpose computers, was not needed for applications that are never to be changed. Air Force approval was required.

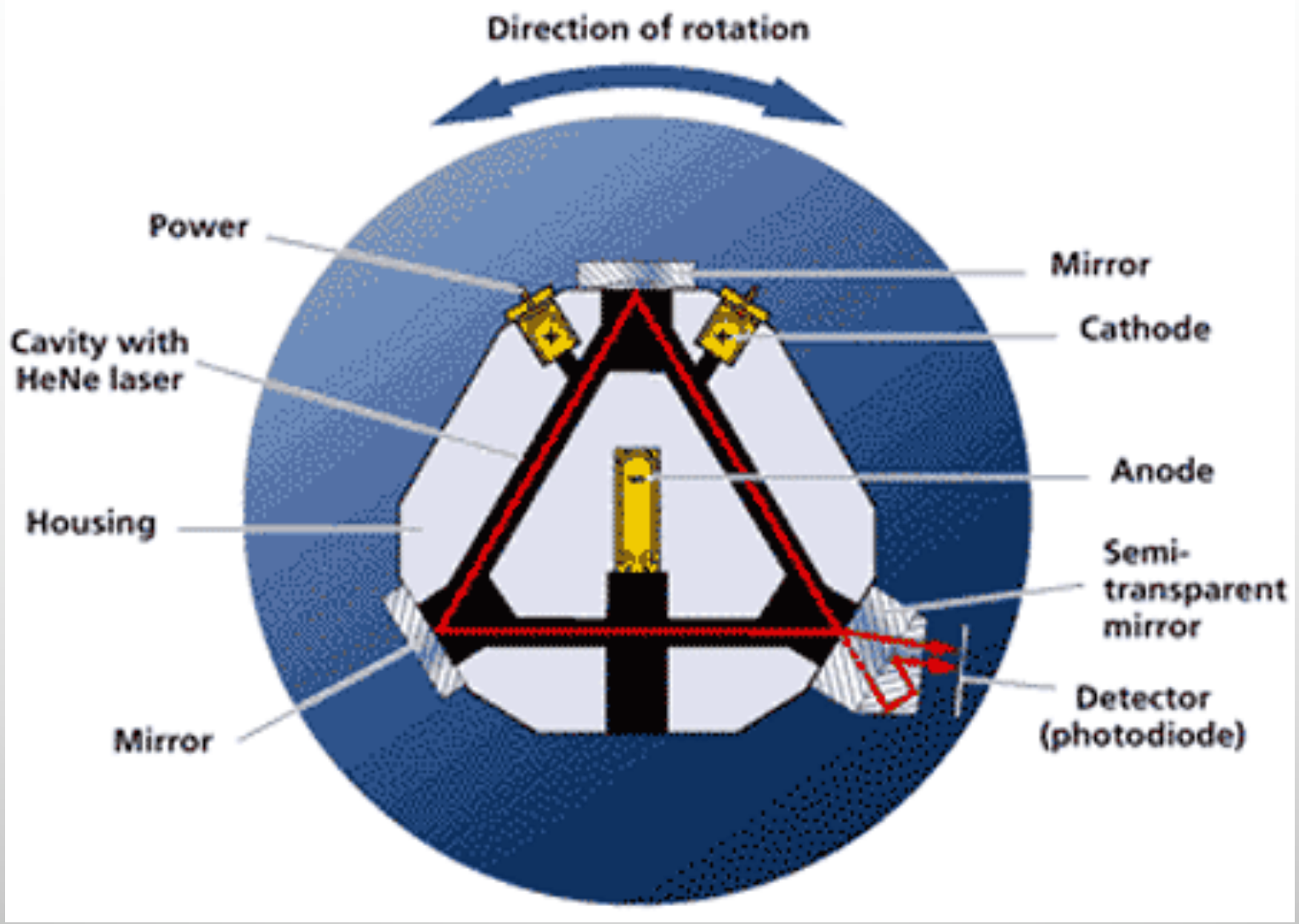
AVIONICS APPLICATION

- The Government also imposed a requirement that all computers, when delivered, operate at no more than 50% speed and memory capacity. This required use of a second 8086, with significant support electronics, and analysis that demonstrated that the program could be properly shared between the 2 processors.

AVIONICS APPLICATION

- **Attitude Motion Detector Systems- AMSS**
- The AMSS performs the function of a ‘rate gyro’, where conditions of instability, are corrected before problems are experienced. The corrections are made at a rate of typically 10 times any aircraft rotation rate- or greater than 100 times per second.
- RLGs (Ring Laser Gyros) were used - 4 total – 3 axes, plus a Redundant unit as the motion sensors.

RING LASER GYRO



AVIONICS APPLICATION

- **B2 Radiation Considerations**
- The aircraft was designed to survive Tactical (as opposed to Strategic) radiation levels that are associated with the Minuteman Missile Silos. The B2 was designed to operate in such environments.
- The less severe tactical levels permitted a dramatic reduction in Semiconductor electronics cost, permitting replacement of Bi-Polar technology (higher power and less dense feature size) with CMOS (Complemtary Metal Oxide Semiconductor) devices.
- A challenge was to design the semiconductor electronics with radiation tolerant devices that were being developed, but not yet in general usage. It was determined that the INTEL CMOS process was considered acceptable for the radiation requirements.

AVIONICS APPLICATION

- The processors recommended and supported by the Government were for more severe requirements but cost over $2000 each. The INTEL 80XX (8086) 16-bit processors were scheduled to start at $230, but eventually $35. Today a unit at least 100 times more powerful and integrated with necessary support electronics can be designed on company rented computer stations, and manufactured in a foundry, with the large quantity unit cost in the dollar range.
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AVIONICS APPLICATION

- B2 Tactical Level Radiation Design Considerations
- All Semiconductors are vulnerable to three types radiation
- **Prompt Gamma** --Upsets digital circuitry (computers, digital logic and inverter power supply control circuits are scrambled)—'Circumvention' is included employing an 'Event Detector'. Critical digital data is continually stored in a 'Hard' memory, and read out subsequent to the event, and resets the devices to resume normal operation.

AVIONICS APPLICATION

- **Total Gamma-** Commercially available CMOS Devices, and Custom designed Analog Microcircuits, must be designed or selected which are tolerant to the specified levels. A Design margin of 10:1 is required with Component testing (Individual or Lot) employed. Radiation Testing facilities and test circuits are required for critical circuitry.
- **Neutron Radiation-** Bipolar transistor and microcircuits are selected with appropriate design margins,
- Detailed Test documentation and results are maintained and verified.

QUESTIONS?